REMARKS/ARGUMENTS

For Priority, Applicant appreciates Examiner's acknowledgment of claim for foreign priority. A certified copy of the Foreign Application has been enclosed in this Office Action response.

The Title of the Invention has been amended per Examiner's suggestion. Applicants believe that the title is sufficiently descriptive of the claimed invention.

For Drawings a replacement sheet has been generated and follows this section of the Response.

For the Specification, changes, where needed, have been made, as noted. However, Applicant respectfully declines Examiner's invitation to add Section Headings. Applicant appreciates the Office Action's suggestion to add section headings to the Specification but respectfully declines the invitation. As noted in the Office Action and also in MPEP § 608.01(a) the suggested section headings are merely preferred and not required. Thus, no amendments adding Section Headings to the disclosure have been presented.

Claims 1-18 remain pending in the present application.

Claim 4 is objected owing to informalities. Claim 16 is objected to under 37 CFR 1.17(c) as being of improper dependent form.

Claims 4 and 16 have been amended to address informalities noted by Examiner.

Claims 18 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite in that it fails to point out what is included or excluded by the claim language.

Claim 18 has been amended to address rejection noted in the Office Action. Applicant believes this claim and other claims comply with §112, second paragraph

Claims 1-4, 9, 10, and 12-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Egerer et al.* (U.S. Patent No. 6,744,304 B2, hereinafter *Egerer*) in view of *Bisping et al.* (U.S. Patent No. 6,726,361B1, hereinafter *Bisping*).

Claims 5, 6, and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Egerer et al.* in view of *Bisping et al.* as applied to claims 1-4, 9, 10, and 12-18, and further in view of Sakurai (U.S. Patent No. 5,993,060A, hereinafter *Sakurai)*

Claims 7 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Egerer et al.* in view of *Bisping et al.* as applied to claims 1-4, 9, 10, and 12-18, and further in view of Morris, Jr. (U.S. Patent No. 4,305,288A, hereinafter *Morris).*

Claims 11 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Egerer et al.* in view of *Bisping et al.* as applied to claims 1-4, 9, 10, and 12-18, and further in view of Tuthill (U.S. Patent No5,982,221A, hereinafter *Tuthill).*

The §103 rejections

The Cited References

Egerer "relates to an electronic circuit for generating an output voltage having a defined temperature dependence. In order to adjust signal transit times, use is frequently made in integrated circuits of time-delay circuits for the purpose of adjusting signals, such as clock signals, for example, to one another. The time-delay circuits serve the purpose, in particular, of making available at each point in the integrated circuits a clock signal that is synchronized with the clock signals that are tapped at other points in the integrated circuit. The time-delay circuits are configured so as to effect a prescribable time delay of the input signal with reference to an output signal. Conventional time delay circuits are, however, temperature-dependent. As a result, the respective signals experience a different time delay as a function of the ambient temperature and/or the junction temperature. The time-delay interval of the time delay circuits is influenced, in particular, during the heating of the integrated circuit as it is being used. Since a plurality of time delay circuits with different time-delay intervals are frequently provided, and since the signal transit times via line lengths are essentially not temperature-dependent, the result of this is that the signals become asynchronous relative to one another. (col. 1, lines 7-30). Furthermore, " the object of the invention to provide an electronic circuit for generating an output voltage having a defined temperature dependence which overcomes the above-mentioned disadvantages of the prior art devices of this general type, and provides a *time-delay circuit* [emphasis added] that makes a temperature-dependent time delay available in a simple way. (col. 1, lines 35-40)."

Bisping has an arrangement for measuring the temperature of an electronic circuit, the arrangement comprising a measuring element being in close thermal communication with the electronic circuit, which measuring element comprises a temperature-dependent component in each one of at least two current paths and whose current-voltage characteristic is dependent on the temperature in accordance with a different predetermined function in at least two of the current paths, which temperature-dependent components can each be impressed with a predetermined current for generating a voltage dependent on the temperature at each one of the temperature-dependent components, and an evaluation circuit for forming an output voltage representing a measure of the temperature of the electronic circuit from the difference of the voltages at the temperature-dependent components. By measuring the output voltage of the arrangement according to the invention, it is possible to measure the instantaneous temperature of the semiconductor body in a simple, rapid and accurate manner. The measured value of the temperature may be directly evaluated by means of an electronic signal processing operation, for example, in an apparatus for performing the pre-measurement.

Applicant's Invention

In contrast with *Egerer*, Applicant's invention addresses a long-felt need for a proportional-to-absolute (PTAT) structure which performs a temperature measurement function without requiring any external diodes and the like. "The demand for low voltage references is especially apparent in mobile battery operated devices, such as cellular phones, pages, camera recorders, and laptops. Consequently, low voltage and low quiescent current low are intrinsic and required characteristics conducive to toward increased battery efficiency and longevity (Specification, page 7, paragraph 6)." Unlike *Egerer*, Applicant's invention is not directed to providing a *time delay* circuit.

An important feature of Applicant's invention "a second stage S2 with p additional CMOS transistors N1 through Np and a resistor $r*R^{temp}$ was introduced (p and r are integers). 1:p and 1:r can be chosen independently from each other. Depending on these ratios, the output voltage level $V_{tempout}$ at the output 17 can be adjusted.

(Specification, page 4, paragraph 2)." Also, the nodes 18 and 19 can be connected to ground, or these nodes 18, 19 can be connected to any desired reference voltage. (Specification, page 4, paragraph 6). These features allow for the scaling of the output voltage $V_{tempout}$ and a shifting of the reference level, without introducing an additional error.

Furthermore, the invention provides the basic PTAT extended by an additional output stage (second stage S2) and an optional temperature compensation network 31. (See Figure 3).

Argument

Claims 1-4, 9, 10, and 12-18

Applicant respectfully asserts that the Office Action fails to make a prima facie case for obviousness under §103(a). The Office Action concedes that *Egerer* does not explicitly teach a parallel arrangement of n diodes and D2 is a parallel arrangement of diodes as claimed by Applicant in Claim 1 (Office Action, page 8, paragraph 2). Furthermore, *Bisping* disclosure of parallel arrangement of "x" diodes is not applicable to Applicant's claimed invention. The combination of *Egerer* of *Bisping* is not proper. Applicant respectfully notes that *Egerer* falls under the U.S. classification of 327/540 and *Bisping* falls under U.S. classification of 374/178. That these two patents are classified in two disparate technology areas does not support the desirability of their combination.

References are not properly combinable or modifiable if their intended function is destroyed. The CCPA and the Federal Circuit have held that when a §103 rejection is based upon a modification of a reference that destroys the intent, purpose or function of the invention disclosed in the reference, such a proposed modification is not proper and the *prima facie* case of obviousness can not be properly made. See *in re Gordon, 733 F. 2d 900, 221 USPQ 1125 (Fed. Cir 1984).* Furthermore, to assert a proper §103 rejection, there must be a basis in the art for combining or modifying references, MPEP §2143.01 provides:

> **The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.** *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)

Alone, or in combination, *Egerer* and *Bisping* does not render obvious, Applicant's claimed features. Consequently, a case for obviousness under §103 has not been made. Applicants request that the §103 rejections be withdrawn. Therefore, claim 1 is allowable and claims dependent therefrom are also allowable.

Claims 5, 6, and 8

Alone *Sukurai,* the artisan in reviewing Applicant's invention would not render it obvious under §103. *Sukurai* "relates generally to a temperature sensor provided with adjusting means for modifying manufacturing variations . . .for use in a temperature-compensated crystal oscillator on small-sized electronic equipment. . .(col. 1, lines 5-10)" Applicant's invention notes that "using identical devices is advisable, because in this way mismatch effects can be reduced to a minimum. Non-ideal effects of the elements will be cancelled by each other (Specification, page 4, paragraph 7)" However, the effectiveness of Applicant's invention is not vitiated if for technical reasons using identical devices is not possible in that the ratios (as mentioned *supra*) of these components determines the inventions performance parameters, i.e. "these equations indicate that the output voltage Vtempout depends only on the ratios p, r, n and the absolute temperature T, but not on any other absolute values (Specification, page 4, paragraph 6)"

In that the combination of *Egerer* and *Bisping* is not sufficient to render Applicant's claimed features obvious the further combination of *Sukurai* is not sufficient, as well. Therefore, claims 5, 6, and 8 as presented are allowable and the §103 rejection should be withdrawn.

Claim 7

Applicant respectfully asserts that *Morris,* "which forward biases a diode sensing element to control the gain of an operational amplifier (Abstract)". In contrast with Applicant's claimed invention which uses a resistor (R_{temp}) to provide a voltage V_{Rtemp}.

The technology in *Morris* would be incompatible with that of Applicant's invention alone or in combination with *Egerer* and *Bisping*. As cited earlier, references are not properly combinable or modifiable if their intended function is destroyed. Thus, the §103 rejection should be withdrawn.

Claim 11

In that the combination of *Egerer* and *Bisping* does not disclose the limitation set forth in claim 11, by not explicitly teaching said operational amplifier is a low-offset operational and is not sufficient to sustain a §103 rejection as argued previously, the combination with *Tuthill* does not make up for the insufficiency. Furthermore, if an independent claim (claim 1) is allowable, claims depending therefrom are also allowable. Applicants requests that the §103 rejection be withdrawn.

Conclusion

Applicant believes he has addressed the Examiner's concerns. Therefore, the claims, as amended, are now allowable over the cited references. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Please charge any fees other than the issue fee and credit any overpayments to Deposit Account 14-1270.

Respectfully submitted,

Date: 24-SEP-2004

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